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Charissa Wheeler

APPLICATION FOR
UNITED STATES LETTERS PATENT

SPECIFICATION

TO ALL WHOM IT MAY CONCERN:

Be it known that I, **Sang Woo NAM**, a citizen of the Republic of Korea, residing at #210-203 Gaesin Jugong 2-cha Apt., Gaesin-dong, Heungdeok-gu, Cheongju-si, Chungcheongbuk-do, 361-709, Korea have invented a new and useful **METHODS FOR FORMING CAPACITORS AND CONTACT HOLES OF SEMICONDUCTOR DEVICES SIMULTANEOUSLY**, of which the following is a specification.

METHODS FOR FORMING CAPACITORS AND CONTACT HOLES OF SEMICONDUCTOR DEVICES SIMULTANEOUSLY

TECHNICAL FIELD

[0001] The present disclosure relates to semiconductor fabrication and, more particularly, to methods for forming capacitors and contact holes of semiconductor devices simultaneously.

BACKGROUND

[0002] In fabricating semiconductor devices or, in particular, analog devices, capacitors must be formed in most cases and a contact hole has to be formed to connect a lower metal layer to another metal line. Generally, the contact hole is formed before or after the formation of the capacitor.

[0003] Figs. 1a and 1b illustrate, in cross-sectional views, a known process for forming a capacitor of a semiconductor device. Referring to Fig. 1a, a metal such as copper or aluminum is deposited on a substrate (not shown) to form a metal line 1'. A titanium nitride (TiN) layer 2' is deposited on the metal line 1'. The TiN layer 2' is used as a lower metal layer of a capacitor. An insulating layer 3' such as oxide or nitride is formed on the TiN layer 2' and an upper metal layer 4' is formed on the insulating layer 3'. Then, a mask layer such as a photoresist pattern 5' is formed on the upper metal layer 4'. Next, some parts of the upper metal layer 4', the insulating layer 3', and the TiN layer 2' are removed by wet or dry etching using the photoresist pattern as a mask. As a result, as shown in Fig. 1b, a capacitor comprising the upper metal layer 4', the insulating layer 3', and the TiN layer 2' is formed on the metal line 1'.

[0004] For example, U.S. Patent No. 6,117,747 to Shao et al. discloses a method for fabricating a metal-oxide capacitor using a dual damascene process. U.S. Patent No. 6,387,775 to Jang et al. discloses a method for forming a metal-insulator-metal (MIM)

capacitor while preserving the dielectric capacitor during the trench etch. As another example, U.S. Patent No. 6,329,234 to Ma et al. discloses a structure and a method for fabricating copper metal-insulator-metal (MIM) capacitors and thick metal inductors simultaneously with only one mask in a damascene and dual damascene trench/via process. High performance device structures formed by Ma et el. patent include: parallel plate capacitor bottom metal (CBM) electrodes and capacitor top metal (CTM) electrodes, MIM capacitors, thick inductor metal wiring, interconnects and contact vias.

[0005] However, if a capacitor and a contact hole are formed separately, the process for manufacturing a semiconductor device become unnecessarily longer and more complicated and probability of defect occurrence increases. In addition, in an etching process, it is difficult to accurately adjust depth and location of etch-stop and conduct process control because both a lower metal layer and a metal line are formed of metals and an etch selectivity of the lower metal layer to the metal line is low.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] Figs. 1a and 1b illustrate, in cross-sectional views, a known process of forming a capacitor of a semiconductor device.

[0007] Figs. 2a and 2b illustrate, in cross-sectional views, the process of forming a capacitor and a contact hole of a semiconductor device simultaneously.

[0008] Fig. 3 is an enlarged view of an area designated with reference numeral 2 in Fig. 2b.

DETAILED DESCRIPTION

[0009] Referring to Figs. 2a and 2b, a metal layer and a titanium nitride (TiN) layer are deposited on a substrate 10 in sequence. A pattern is formed on the TiN layer and some parts of the metal layer and the TiN layer are removed through the pattern to form a capacitor part comprising a metal layer 11 and a TiN layer 12 and a contact hole part comprising a metal layer 21 and a TiN layer 22. The metal layers 11 and 21 may be formed of Al, Al/Cu alloy, Cu, etc. The TiN layers 12 and 22 may be formed through plasma sputtering using a Ti target.

[0010] Then, an insulating layer 31 with an appropriate thickness is formed over the substrate 10 including the capacitor part and the contact hole part. An interlayer dielectric (ILD) layer 32, which is thicker than the insulating layer 31, is formed on the insulating layer. In one example, t/he insulating layer 31 is formed of nitride (e.g., Si_3N_4) to prevent short circuiting between the metal layers 11 and 12 and other metal layers formed later. To grow the nitride, materials such as NH_3, SiH_2Cl_2, etc. are generally used. The ILD layer 32 is formed of a material with a low dielectric constant such as, for example, silica or fluorinated silica glass (FSG, SiO_xF_y).

[0011] Next, a first photoresist pattern 33 with windows 33a and 33b is formed on the ILD layer 32. A first etching process is performed using the first photoresist pattern 33 as a mask. Some parts of the ILD layer 32 under the windows 33a and 33b are removed to form openings on the insulating layer 31. Here, a reactive ion etching (RIE) etcher may be used as etching equipment. Then, a second photoresist pattern 34 with a window 34b is formed on the ILD layer 32 including the openings. A second etching process is performed using the second photoresist pattern 34 as a mask. As a result, some part of the insulating layer 31 and the TiN layer 22 under the windows 34b are removed and, therefore, the opening in the contact hole part is extended to the metal layer 21. In the second etching process, the

insulating layer 31 is etched using CHF_3, NF_3, or SiF_4 as an etching gas and the TiN layer 22 is etched through an RIE process using HF as an etching gas.

[0012] The second photoresist pattern 34 is removed and, then, the openings formed through the first and second etching processes are filled with tungsten to form tungsten plugs. In forming the tungsten plugs, preferably as in a damascene process, the tungsten is deposited over the ILD layer including the openings and planarized by a CMP (Chemical Mechanical Polishing) process. Through such damascene process, device defects can be minimized.

[0013] Fig. 3 is an enlarged view of a capacitor shown in 2 of Fig. 2b. The capacitor comprises the metal layer 11 as a lower metal layer, the insulating layer 31, i.e., nitride, as a capacitor dielectric layer related to capacitance, and the tungsten plug 35 as an upper metal layer.

[0014] Therefore, a capacitor as disclosed herein may comprise the metal layer as a lower metal layer, the insulating layer, and the tungsten plug as an upper metal layer. In addition, a capacitor as disclosed herein may use the TiN layer as a lower metal layer without forming a separate lower metal layer.

[0015] As disclosed above, a method for fabricating a semiconductor device simplifies processes by forming a capacitor and a contact hole substantially simultaneously. Additionally, as disclosed above, a method is provided for fabricating a semiconductor device that can easily control processes using one layer constituting a capacitor as an etch-stop layer. Accordingly, the disclosed methods and apparatus can reduce device defects by forming the upper metal layer of capacitor through a damascene process and prevent short circuit between the metal layer and the tungsten by protecting the metal layer using the insulating layer, i.e., nitride. In addition, as disclosed herein a semiconductor device may be fabricated with a

simple structure by using the tungsten plug, which connects metal lines, as an upper metal layer of a capacitor.

[0016] Although certain apparatus constructed in accordance with the teachings of the invention have been described herein, the scope of coverage of this patent is not limited thereto. On the contrary, this patent covers every apparatus, method and article of manufacture fairly falling within the scope of the appended claims either literally or under the doctrine of equivalents.